```
RCS file: /s6/cvsroot/euterpe/BOM,v
Working file: BOM
head: 5.105
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1940;  selected revisions: 15
description:
top level BOM
----------------------------
revision 3.866
date: 1995/06/23 02:32:52;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc

consolidate routing congestion changes. latest base files.  stop after
linesearch
----------------------------
revision 3.865
date: 1995/06/22 22:31:36;  author: jeffm;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify
      Makerules.local

Removed local rule for making .in files.
----------------------------
revision 3.864
date: 1995/06/22 18:57:36;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/hc

avoid toplevel collisions
----------------------------
revision 3.863
date: 1995/06/22 18:56:21;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/rg

avoid toplevel collisions
----------------------------
revision 3.862
date: 1995/06/21 21:54:34;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/hc

placement change to avoid toplevel collisions
----------------------------
revision 3.861
date: 1995/06/21 21:50:12;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/rg

placement change to avoid toplevel collisions
----------------------------
revision 3.860
date: 1995/06/21 20:52:29;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/cp

placement change to avoid toplevel collisions
----------------------------
revision 3.859
```

```
date: 1995/06/21 20:48:18;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/au

placement change to avoid toplevel collisions
----------------------------
revision 3.858
date: 1995/06/21 17:23:11;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/es

eliminate 64 wires in conjested area
----------------------------
revision 3.857
date: 1995/06/21 07:34:39;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/uu

uu/uu.V:  Single end many of the instU* and preemdInstU* busses on the bits
  already being forced fullswing by other logic or when halfswing loading
  seemed light enough to not make the power-up risk high.  Rqstd by dickson.
  Explicitly called out vref_0ph in some concatenations so that old .pim works.
----------------------------
revision 3.856
date: 1995/06/20 23:56:15;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/rg

move lower data path section to the right to make room for es growth
----------------------------
revision 3.855
date: 1995/06/20 23:08:40;  author: jeffm;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/toplevel

Make new tests available:

      readdaemon
      scasdep
      cerbtotest
      hermtotest
----------------------------
revision 3.854
date: 1995/06/20 22:09:18;  author: woody;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/hc

hc_brresp.pla, hc.h: Simplified event daemon prb processing since it was
possible that the prb repsonse could be granted before ostate loaded the tag
into the sid[7] tag register. This was noticed by standalone test gauntlet
(CPUCLK=13, IOCLK=8). Saves ~70 hopper atoms (as reported by planet).

The result is that Event Daemon stores will take longer to release the nb entry.
No placement change required.

Passed multiple standalone tests: gauntlet, termite, hexratio, evnt8
----------------------------
revision 3.853
date: 1995/06/20 05:19:06;  author: woody;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/hc

Only allow tagen[7] when set is active to prevent writing event daemon tag with
bogus value. Standalone test gauntlet detected problem.
```

```
----------------------------
revision 3.852
date: 1995/06/20 00:01:23;  author: jeffm;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/toplevel/hermes

Fix I1 versions of test
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/BOM,v
Working file: verify/BOM
head: 12.34
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 404;   selected revisions: 3
description:
----------------------------
revision 4.189
date: 1995/06/22 22:31:16;  author: jeffm;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify
      Makerules.local

Removed local rule for making .in files.
----------------------------
revision 4.188
date: 1995/06/20 23:08:18;  author: jeffm;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/toplevel

Make new tests available:

      readdaemon
      scasdep
      cerbtotest
      hermtotest
----------------------------
revision 4.187
date: 1995/06/20 00:01:02;  author: jeffm;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/toplevel/hermes

Fix I1 versions of test
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/Makerules.local,v
Working file: verify/Makerules.local
head: 3.16
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 16;    selected revisions: 1
description:
----------------------------
revision 3.13
date: 1995/06/22 22:30:23;  author: jeffm;  state: Exp;  lines: +1 -7
Remove special rule for making .in files - the standard .in file
is ok.
```

```
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/obj/processor/inst/Makefile,v
Working file: verify/obj/processor/inst/Makefile
head: 1.182
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 182;   selected revisions: 3
description:
----------------------------
revision 1.169
date: 1995/06/20 22:57:32;  author: jeffm;  state: Exp;  lines: +3 -3
Hermes and cerberus timeout machine check tests. Neither are able
to be run on hwterp.

cerbtotest causes one machine check
hermtotest causes three machine checks
----------------------------
revision 1.168
date: 1995/06/20 21:07:04;  author: jeffm;  state: Exp;  lines: +3 -2
Test that reading the event daemon is not destructive. Expect it to
act like a normal load.
----------------------------
revision 1.167
date: 1995/06/20 20:37:19;  author: jeffm;  state: Exp;  lines: +2 -2
Test register dependencies and compare and swap.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/perf/cerb_perf.S,v
Working file: verify/perf/cerb_perf.S
head: 1.7
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 7;     selected revisions: 1
description:
----------------------------
revision 1.5
date: 1995/06/21 18:31:13;  author: claseman;  state: Exp;  lines: +15 -10
some fine tuning changes
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/perf/perflog.srl,v
Working file: verify/perf/perflog.srl
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.1
date: 1995/06/22 23:01:02;  author: jeffm;  state: Exp;
```

```
Standard log to analyse performance.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r4356.S,v
Working file: verify/random/regdepend_r4356.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.1
date: 1995/06/20 14:18:21;  author: dit00;  state: Exp;
New test, ran ok
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r4552.S,v
Working file: verify/random/regdepend_r4552.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.1
date: 1995/06/19 16:52:48;  author: dit00;  state: Exp;
Add new test,ran ok
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r4752.S,v
Working file: verify/random/regdepend_r4752.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.1
date: 1995/06/19 16:53:23;  author: dit00;  state: Exp;
Add new test,ran ok
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r4951.S,v
Working file: verify/random/regdepend_r4951.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
```

```
----------------------------
revision 3.1
date: 1995/06/19 16:53:57;  author: dit00;  state: Exp;
Add new test,ran ok
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r5152.S,v
Working file: verify/random/regdepend_r5152.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.1
date: 1995/06/19 16:54:33;  author: dit00;  state: Exp;
Add new test,ran ok
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r5352.S,v
Working file: verify/random/regdepend_r5352.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.1
date: 1995/06/19 16:54:51;  author: dit00;  state: Exp;
Add new test,ran ok
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/hc/nbhc_drive.V,v
Working file: verify/standalone/hc/nbhc_drive.V
head: 1.55
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 55;    selected revisions: 1
description:
----------------------------
revision 1.53
date: 1995/06/20 21:46:49;  author: brian;  state: Exp;  lines: +17 -16
Changed output pbb/prb output format.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/hc/parseout,v
Working file: verify/standalone/hc/parseout
head: 7.4
branch:
locks: strict
access list:
```

```
keyword substitution: kv
total revisions: 4;     selected revisions: 1
description:
----------------------------
revision 7.4
date: 1995/06/20 21:46:52;  author: brian;  state: Exp;  lines: +3 -3
Changed output pbb/prb output format.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/hc/termite2.vec,v
Working file: verify/standalone/hc/termite2.vec
head: 10.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 2
description:
----------------------------
revision 10.2
date: 1995/06/20 21:46:54;  author: brian;  state: Exp;  lines: +13 -209
Changed output pbb/prb output format.
----------------------------
revision 10.1
date: 1995/06/19 18:20:48;  author: brian;  state: Exp;
Trying to hit a version of the bug.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/io/verdrive.V,v
Working file: verify/standalone/io/verdrive.V
head: 1.15
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 15;    selected revisions: 1
description:
----------------------------
revision 1.15
date: 1995/06/21 23:28:12;  author: brian;  state: Exp;  lines: +3 -2
Updated driver for hcdisOUT and differential reset.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/BOM,v
Working file: verify/toplevel/BOM
head: 44.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 132;   selected revisions: 3
description:
releasebom adding BOM
----------------------------
revision 40.0
date: 1995/06/20 23:08:05;  author: jeffm;  state: Exp;  lines: +1 -1
Release Target: euterpe/verify/toplevel
```

```
Make new tests available:

      readdaemon
      scasdep
      cerbtotest
      hermtotest
----------------------------
revision 39.43
date: 1995/06/20 23:07:56;  author: jeffm;  state: Exp;  lines: +20 -37
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 39.42
date: 1995/06/20 00:00:49;  author: jeffm;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/toplevel/hermes

Fix I1 versions of test
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/Makefile,v
Working file: verify/toplevel/Makefile
head: 1.185
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 185;   selected revisions: 3
description:
----------------------------
revision 1.169
date: 1995/06/20 22:57:32;  author: jeffm;  state: Exp;  lines: +3 -3
Hermes and cerberus timeout machine check tests. Neither are able
to be run on hwterp.

cerbtotest causes one machine check
hermtotest causes three machine checks
----------------------------
revision 1.168
date: 1995/06/20 21:07:04;  author: jeffm;  state: Exp;  lines: +3 -2
Test that reading the event daemon is not destructive. Expect it to
act like a normal load.
----------------------------
revision 1.167
date: 1995/06/20 20:37:19;  author: jeffm;  state: Exp;  lines: +2 -2
Test register dependencies and compare and swap.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/cerbtotest.S,v
Working file: verify/toplevel/cerbtotest.S
head: 39.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
```

```
revision 39.1
date: 1995/06/20 22:57:29;  author: jeffm;  state: Exp;
Hermes and cerberus timeout machine check tests. Neither are able
to be run on hwterp.

cerbtotest causes one machine check
hermtotest causes three machine checks
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/hermtotest.S,v
Working file: verify/toplevel/hermtotest.S
head: 39.5
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 5;     selected revisions: 1
description:
----------------------------
revision 39.1
date: 1995/06/20 22:57:25;  author: jeffm;  state: Exp;
Hermes and cerberus timeout machine check tests. Neither are able
to be run on hwterp.

cerbtotest causes one machine check
hermtotest causes three machine checks
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/hermtotest.hconfig,v
Working file: verify/toplevel/hermtotest.hconfig
head: 39.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;     selected revisions: 1
description:
----------------------------
revision 39.1
date: 1995/06/20 22:57:22;  author: jeffm;  state: Exp;
Hermes and cerberus timeout machine check tests. Neither are able
to be run on hwterp.

cerbtotest causes one machine check
hermtotest causes three machine checks
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/readdaemon.S,v
Working file: verify/toplevel/readdaemon.S
head: 39.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;     selected revisions: 1
description:
----------------------------
```

```
revision 39.1
date: 1995/06/20 21:07:08;  author: jeffm;  state: Exp;
Test that reading the event daemon is not destructive. Expect it to
act like a normal load.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/scasdep.S,v
Working file: verify/toplevel/scasdep.S
head: 39.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;     selected revisions: 1
description:
----------------------------
revision 39.1
date: 1995/06/20 20:37:21;  author: jeffm;  state: Exp;
Test register dependencies and compare and swap.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/hermes/BOM,v
Working file: verify/toplevel/hermes/BOM
head: 12.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 22;    selected revisions: 2
description:
releasebom adding BOM
----------------------------
revision 11.0
date: 1995/06/20 00:00:37;  author: jeffm;  state: Exp;  lines: +1 -1
Release Target: euterpe/verify/toplevel/hermes

Fix I1 versions of test
----------------------------
revision 10.1
date: 1995/06/20 00:00:27;  author: jeffm;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/hermes/hermestest.S,v
Working file: verify/toplevel/hermes/hermestest.S
head: 1.8
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 8;     selected revisions: 1
description:
----------------------------
revision 1.8
date: 1995/06/19 23:59:37;  author: jeffm;  state: Exp;  lines: +18 -18
Initialize all tag entries - uninit'd tags causing I1 versions
of test to fail.
```

```
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/BOM,v
Working file: verilog/BOM
head: 6.9
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1390;  selected revisions: 12
description:
top level verilog BOM
----------------------------
revision 3.640
date: 1995/06/23 02:32:34;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc

consolidate routing congestion changes. latest base files.  stop after
linesearch
----------------------------
revision 3.639
date: 1995/06/22 18:57:15;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/hc

avoid toplevel collisions
----------------------------
revision 3.638
date: 1995/06/22 18:55:59;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/rg

avoid toplevel collisions
----------------------------
revision 3.637
date: 1995/06/21 21:54:14;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/hc

placement change to avoid toplevel collisions
----------------------------
revision 3.636
date: 1995/06/21 21:49:47;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/rg

placement change to avoid toplevel collisions
----------------------------
revision 3.635
date: 1995/06/21 20:52:06;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/cp

placement change to avoid toplevel collisions
----------------------------
revision 3.634
date: 1995/06/21 20:47:56;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/au

placement change to avoid toplevel collisions
----------------------------
revision 3.633
```

```
date: 1995/06/21 17:22:55;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/es

eliminate 64 wires in conjested area
----------------------------
revision 3.632
date: 1995/06/21 07:34:21;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/uu

uu/uu.V:  Single end many of the instU* and preemdInstU* busses on the bits
  already being forced fullswing by other logic or when halfswing loading
  seemed light enough to not make the power-up risk high.  Rqstd by dickson.
  Explicitly called out vref_0ph in some concatenations so that old .pim works.
----------------------------
revision 3.631
date: 1995/06/20 23:55:52;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/rg

move lower data path section to the right to make room for es growth
----------------------------
revision 3.630
date: 1995/06/20 22:08:53;  author: woody;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/hc

hc_brresp.pla, hc.h: Simplified event daemon prb processing since it was
possible that the prb repsonse could be granted before ostate loaded the tag
into the sid[7] tag register. This was noticed by standalone test gauntlet
(CPUCLK=13, IOCLK=8). Saves ~70 hopper atoms (as reported by planet).

The result is that Event Daemon stores will take longer to release the nb entry.
No placement change required.

Passed multiple standalone tests: gauntlet, termite, hexratio, evnt8
----------------------------
revision 3.629
date: 1995/06/20 05:18:49;  author: woody;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/hc

Only allow tagen[7] when set is active to prevent writing event daemon tag with
bogus value. Standalone test gauntlet detected problem.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/BOM,v
Working file: verilog/bsrc/BOM
head: 346.6
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1737;  selected revisions: 13
description:
----------------------------
revision 324.0
date: 1995/06/23 02:32:15;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc
```

```
consolidate routing congestion changes. latest base files.  stop after
linesearch
----------------------------
revision 323.12
date: 1995/06/23 02:32:02;  author: tbr;  state: Exp;  lines: +14 -14
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 323.11
date: 1995/06/22 18:56:56;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/hc

avoid toplevel collisions
----------------------------
revision 323.10
date: 1995/06/22 18:55:36;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/rg

avoid toplevel collisions
----------------------------
revision 323.9
date: 1995/06/21 21:53:54;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/hc

placement change to avoid toplevel collisions
----------------------------
revision 323.8
date: 1995/06/21 21:49:27;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/rg

placement change to avoid toplevel collisions
----------------------------
revision 323.7
date: 1995/06/21 20:51:45;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/cp

placement change to avoid toplevel collisions
----------------------------
revision 323.6
date: 1995/06/21 20:47:38;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/au

placement change to avoid toplevel collisions
----------------------------
revision 323.5
date: 1995/06/21 17:22:41;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/es

eliminate 64 wires in conjested area
----------------------------
revision 323.4
date: 1995/06/21 07:34:04;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/uu

uu/uu.V:  Single end many of the instU* and preemdInstU* busses on the bits
  already being forced fullswing by other logic or when halfswing loading
  seemed light enough to not make the power-up risk high.  Rqstd by dickson.
  Explicitly called out vref_0ph in some concatenations so that old .pim works.
```

```
----------------------------
revision 323.3
date: 1995/06/20 23:55:32;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/rg

move lower data path section to the right to make room for es growth
----------------------------
revision 323.2
date: 1995/06/20 22:08:27;  author: woody;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/hc

hc_brresp.pla, hc.h: Simplified event daemon prb processing since it was
possible that the prb repsonse could be granted before ostate loaded the tag
into the sid[7] tag register. This was noticed by standalone test gauntlet
(CPUCLK=13, IOCLK=8). Saves ~70 hopper atoms (as reported by planet).

The result is that Event Daemon stores will take longer to release the nb entry.
No placement change required.

Passed multiple standalone tests: gauntlet, termite, hexratio, evnt8
----------------------------
revision 323.1
date: 1995/06/20 05:18:34;  author: woody;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/hc

Only allow tagen[7] when set is active to prevent writing event daemon tag with
bogus value. Standalone test gauntlet detected problem.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/Makefile.tst,v
Working file: verilog/bsrc/Makefile.tst
head: 40.104
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 104;   selected revisions: 1
description:
----------------------------
revision 40.85
date: 1995/06/19 05:55:35;  author: tbr;  state: Exp;  lines: +7 -7
slight tweak to all.net ordering function
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/chip_euterpe-base.netcap,v
Working file: verilog/bsrc/chip_euterpe-base.netcap
head: 312.20
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 20;    selected revisions: 1
description:
----------------------------
revision 312.3
date: 1995/06/23 02:13:32;  author: tbr;  state: Exp;  lines: +17108 -17318
latest base files.  stop after linesearch
```

```
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/chip_euterpe-base.nof,v
Working file: verilog/bsrc/chip_euterpe-base.nof
head: 307.11
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 11;    selected revisions: 1
description:
----------------------------
revision 307.6
date: 1995/06/23 02:17:17;  author: tbr;  state: Exp;  lines: +88303 -88370
latest base files.  stop after linesearch
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/chip_euterpe-base.pim,v
Working file: verilog/bsrc/chip_euterpe-base.pim
head: 312.23
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 23;    selected revisions: 1
description:
----------------------------
revision 312.3
date: 1995/06/23 02:20:40;  author: tbr;  state: Exp;  lines: +2848 -2681
latest base files.  stop after linesearch
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/chip_euterpe-base.strength,v
Working file: verilog/bsrc/chip_euterpe-base.strength
head: 312.20
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 20;    selected revisions: 1
description:
----------------------------
revision 312.3
date: 1995/06/23 02:21:42;  author: tbr;  state: Exp;  lines: +2213 -2106
latest base files.  stop after linesearch
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/chip_euterpe-base.xrf,v
Working file: verilog/bsrc/chip_euterpe-base.xrf
head: 307.11
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 11;    selected revisions: 1
description:
----------------------------
```

```
revision 307.6
date: 1995/06/23 02:23:01;  author: tbr;  state: Exp;  lines: +52099 -52153
latest base files.  stop after linesearch
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/euterpe.V,v
Working file: verilog/bsrc/euterpe.V
head: 6.431
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 431;   selected revisions: 1
description:
----------------------------
revision 6.426
date: 1995/06/19 18:23:11;  author: dickson;  state: Exp;  lines: +10 -7
single ended return snake bus path from cp to gt. this saves 32 vertical
wires in cp and 32 wires into gt from cp.

also saved 98 wires from cp to cerberus for snake bus wdata data and
address. vref generators were adedd to cp to accomplish this.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/euterpe.status,v
Working file: verilog/bsrc/euterpe.status
head: 24.83
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 83;    selected revisions: 1
description:
----------------------------
revision 24.75
date: 1995/06/19 18:26:19;  author: billz;  state: Exp;  lines: +3 -1
Noted there's a bug in DR/DRIO for ratio=4 (ratiom1=3).
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/padtiles.ercf,v
Working file: verilog/bsrc/padtiles.ercf
head: 168.8
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 8;     selected revisions: 2
description:
----------------------------
revision 168.6
date: 1995/06/23 02:24:19;  author: tbr;  state: Exp;  lines: +9 -9
latest base files.  stop after linesearch
----------------------------
revision 168.5
date: 1995/06/19 05:44:05;  author: tbr;  state: Exp;  lines: +1 -1
take all.net file in order given
=============================================================================
```

```
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/au/BOM,v
Working file: verilog/bsrc/au/BOM
head: 44.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 89;    selected revisions: 2
description:
----------------------------
revision 44.0
date: 1995/06/21 20:47:16;  author: dickson;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/au

placement change to avoid toplevel collisions
----------------------------
revision 43.1
date: 1995/06/21 20:47:09;  author: dickson;  state: Exp;  lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/au/Makefile,v
Working file: verilog/bsrc/au/Makefile
head: 1.11
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 11;    selected revisions: 1
description:
----------------------------
revision 1.11
date: 1995/06/21 20:46:23;  author: dickson;  state: Exp;  lines: +5 -2
updated placement to avoid toplevel collisions
also disabled pifpak as cells were moving
unpredictably
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/au/auindx.pim,v
Working file: verilog/bsrc/au/auindx.pim
head: 12.11
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 11;    selected revisions: 1
description:
----------------------------
revision 12.11
date: 1995/06/21 20:46:25;  author: dickson;  state: Exp;  lines: +308 -308
updated placement to avoid toplevel collisions
also disabled pifpak as cells were moving
unpredictably
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/BOM,v
```

```
Working file: verilog/bsrc/ce/BOM
head: 86.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 170;   selected revisions: 2
description:
releasebom adding BOM
----------------------------
revision 81.0
date: 1995/06/23 02:26:23;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

consolidate routing congestion changes. latest base files.  stop after
linesearch
----------------------------
revision 80.1
date: 1995/06/23 02:26:16;  author: tbr;  state: Exp;  lines: +4 -4
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/ce_cms2ecl.V,v
Working file: verilog/bsrc/ce/ce_cms2ecl.V
head: 2.24
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 24;    selected revisions: 2
description:
----------------------------
revision 2.20
date: 1995/06/21 00:42:42;  author: dickson;  state: Exp;  lines: +2 -2
bad index on addressvref signal
----------------------------
revision 2.19
date: 1995/06/19 18:05:06;  author: dickson;  state: Exp;  lines: +118 -116
added vref connections for address and write data from cp to cerberus.
this saves 98 wires between the top of cp to cerberus.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/cerberus.V,v
Working file: verilog/bsrc/ce/cerberus.V
head: 1.63
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 63;    selected revisions: 1
description:
----------------------------
revision 1.55
date: 1995/06/19 18:05:08;  author: dickson;  state: Exp;  lines: +8 -6
added vref connections for address and write data from cp to cerberus.
this saves 98 wires between the top of cp to cerberus.
=============================================================================
```

```
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/cerbtest.V,v
Working file: verilog/bsrc/ce/cerbtest.V
head: 1.46
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 46;    selected revisions: 1
description:
----------------------------
revision 1.42
date: 1995/06/19 18:05:11;  author: dickson;  state: Exp;  lines: +5 -3
added vref connections for address and write data from cp to cerberus.
this saves 98 wires between the top of cp to cerberus.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cj/BOM,v
Working file: verilog/bsrc/cj/BOM
head: 122.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 259;   selected revisions: 2
description:
----------------------------
revision 121.0
date: 1995/06/23 02:26:53;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

consolidate routing congestion changes. latest base files.  stop after
linesearch
----------------------------
revision 120.1
date: 1995/06/23 02:26:46;  author: tbr;  state: Exp;  lines: +2 -1
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cj/brxcdefer.tst,v
Working file: verilog/bsrc/cj/brxcdefer.tst
head: 120.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 120.1
date: 1995/06/20 21:24:37;  author: mws;  state: Exp;
New br-detected deferred-to-trgt I prblm (also BHicMid) test.
  Not quite right yet.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cp/BOM,v
Working file: verilog/bsrc/cp/BOM
```

```
head: 60.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 119;   selected revisions: 2
description:
releasebom adding BOM
----------------------------
revision 59.0
date: 1995/06/21 20:51:23;  author: dickson;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/cp

placement change to avoid toplevel collisions
----------------------------
revision 58.1
date: 1995/06/21 20:51:15;  author: dickson;  state: Exp;  lines: +6 -6
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cp/cp.V,v
Working file: verilog/bsrc/cp/cp.V
head: 1.39
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 39;    selected revisions: 1
description:
----------------------------
revision 1.35
date: 1995/06/19 18:24:58;  author: dickson;  state: Exp;  lines: +37 -7
single ended connections to cerberus and gt. saves 130 wires total.
placement changes are required  but not checked int yet.
placement updates to follow sometime today.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cp/cph.pim,v
Working file: verilog/bsrc/cp/cph.pim
head: 41.8
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 8;     selected revisions: 1
description:
----------------------------
revision 41.8
date: 1995/06/21 20:50:31;  author: dickson;  state: Exp;  lines: +9 -9
placement change to avoid toplevel collisions
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cp/cphh.pim,v
Working file: verilog/bsrc/cp/cphh.pim
head: 47.4
branch:
locks: strict
```

```
access list:
keyword substitution: kv
total revisions: 4;     selected revisions: 1
description:
----------------------------
revision 47.3
date: 1995/06/19 19:11:50;  author: dickson;  state: Exp;  lines: +14 -0
added placement fixups for earlier conjestion fix.
single ended connection for snake return data path
from cp to gt. also single ended/vref change for
write data and address from cp to cerberus.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cp/cpl.pim,v
Working file: verilog/bsrc/cp/cpl.pim
head: 41.7
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 7;     selected revisions: 1
description:
----------------------------
revision 41.7
date: 1995/06/19 19:11:53;  author: dickson;  state: Exp;  lines: +33 -0
added placement fixups for earlier conjestion fix.
single ended connection for snake return data path
from cp to gt. also single ended/vref change for
write data and address from cp to cerberus.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cp/power.tab.local,v
Working file: verilog/bsrc/cp/power.tab.local
head: 5.15
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 15;    selected revisions: 1
description:
----------------------------
revision 5.15
date: 1995/06/19 21:53:50;  author: dickson;  state: Exp;  lines: +34 -34
power level forces needed fortoday's earlier logic changes.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/es/BOM,v
Working file: verilog/bsrc/es/BOM
head: 97.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 198;   selected revisions: 2
description:
----------------------------
revision 95.0
```

```
date: 1995/06/21 17:22:25;  author: dickson;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/es

eliminate 64 wires in conjested area
----------------------------
revision 94.1
date: 1995/06/21 17:22:18;  author: dickson;  state: Exp;  lines: +5 -5
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/es/es.V,v
Working file: verilog/bsrc/es/es.V
head: 5.46
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 46;    selected revisions: 1
description:
----------------------------
revision 5.46
date: 1995/06/21 17:20:48;  author: dickson;  state: Exp;  lines: +13 -3
elliminate 64 wires that cross from lower data path to lower
data path. had to add 64 buf_1's to accomplish this.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/es/es.pim,v
Working file: verilog/bsrc/es/es.pim
head: 5.55
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 55;    selected revisions: 1
description:
----------------------------
revision 5.54
date: 1995/06/21 17:21:12;  author: dickson;  state: Exp;  lines: +67 -3
elliminate 64 wires that cross from lower data path to lower
data path. had to add 64 buf_1's to accomplish this.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/es/esaddbyt.V,v
Working file: verilog/bsrc/es/esaddbyt.V
head: 1.18
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 18;    selected revisions: 1
description:
----------------------------
revision 1.17
date: 1995/06/21 17:21:23;  author: dickson;  state: Exp;  lines: +2 -2
elliminate 64 wires that cross from lower data path to lower
data path. had to add 64 buf_1's to accomplish this.
=============================================================================
```

```
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/es/esaddbyta.V,v
Working file: verilog/bsrc/es/esaddbyta.V
head: 60.6
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 6;     selected revisions: 1
description:
----------------------------
revision 60.5
date: 1995/06/21 17:21:25;  author: dickson;  state: Exp;  lines: +2 -2
elliminate 64 wires that cross from lower data path to lower
data path. had to add 64 buf_1's to accomplish this.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/gt/BOM,v
Working file: verilog/bsrc/gt/BOM
head: 98.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 194;   selected revisions: 2
description:
releasebom adding BOM
----------------------------
revision 97.0
date: 1995/06/23 02:28:49;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

consolidate routing congestion changes. latest base files.  stop after
linesearch
----------------------------
revision 96.1
date: 1995/06/23 02:28:42;  author: tbr;  state: Exp;  lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/gt/gt.V,v
Working file: verilog/bsrc/gt/gt.V
head: 2.28
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 28;    selected revisions: 1
description:
----------------------------
revision 2.28
date: 1995/06/19 18:20:03;  author: dickson;  state: Exp;  lines: +5 -4
single ended return snake bus path from cp
input   [31:0]  CEprbi; // from cerb

no placement necessary
=============================================================================
```

```
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/gt/gtsnake.V,v
Working file: verilog/bsrc/gt/gtsnake.V
head: 7.41
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 41;    selected revisions: 2
description:
----------------------------
revision 7.41
date: 1995/06/19 23:21:30;  author: dickson;  state: Exp;  lines: +5 -5
tried to single end input to dor2 and hooked a vref to a select input.
swapped order of two input pairs  to get around this.
----------------------------
revision 7.40
date: 1995/06/19 18:26:34;  author: dickson;  state: Exp;  lines: +8 -7
forgot this in my last checkin for single ending cp to gt
snake bus return data path.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hc/BOM,v
Working file: verilog/bsrc/hc/BOM
head: 125.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 250;   selected revisions: 8
description:
releasebom adding BOM
----------------------------
revision 115.0
date: 1995/06/22 18:56:34;  author: dickson;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/hc

avoid toplevel collisions
----------------------------
revision 114.1
date: 1995/06/22 18:56:24;  author: dickson;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 114.0
date: 1995/06/21 21:53:26;  author: dickson;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/hc

placement change to avoid toplevel collisions
----------------------------
revision 113.1
date: 1995/06/21 21:53:17;  author: dickson;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 113.0
date: 1995/06/20 22:08:08;  author: woody;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/hc
```

```
hc_brresp.pla, hc.h: Simplified event daemon prb processing since it was
possible that the prb repsonse could be granted before ostate loaded the tag
into the sid[7] tag register. This was noticed by standalone test gauntlet
(CPUCLK=13, IOCLK=8). Saves ~70 hopper atoms (as reported by planet).

The result is that Event Daemon stores will take longer to release the nb entry.
No placement change required.

Passed multiple standalone tests: gauntlet, termite, hexratio, evnt8
----------------------------
revision 112.1
date: 1995/06/20 22:08:00;  author: woody;  state: Exp;  lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 112.0
date: 1995/06/20 05:18:18;  author: woody;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/hc

Only allow tagen[7] when set is active to prevent writing event daemon tag with
bogus value. Standalone test gauntlet detected problem.
----------------------------
revision 111.1
date: 1995/06/20 05:18:11;  author: woody;  state: Exp;  lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hc/hc.V,v
Working file: verilog/bsrc/hc/hc.V
head: 1.56
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 56;    selected revisions: 1
description:
----------------------------
revision 1.54
date: 1995/06/20 05:05:26;  author: woody;  state: Exp;  lines: +2 -2
Modified a comment.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hc/hc.h,v
Working file: verilog/bsrc/hc/hc.h
head: 3.15
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 15;    selected revisions: 1
description:
----------------------------
revision 3.15
date: 1995/06/20 21:56:21;  author: woody;  state: Exp;  lines: +5 -7
hc_brresp.pla, hc.h: Simplified event daemon prb processing since it was
possible that the prb repsonse could be granted before ostate loaded the tag
into the sid[7] tag register. This was noticed by standalone test gauntlet
(CPUCLK=13, IOCLK=8). Saves ~70 hopper atoms (as reported by planet).
```

. . . .

```
No placement change required.

Passed multiple standalone tests: gauntlet, termite, hexratio, evnt8
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hc/hc0_control.pim,v
Working file: verilog/bsrc/hc/hc0_control.pim
head: 73.25
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 25;    selected revisions: 2
description:
----------------------------
revision 73.20
date: 1995/06/22 18:55:45;  author: dickson;  state: Exp;  lines: +4 -7
avoid toplevel collisions
----------------------------
revision 73.19
date: 1995/06/21 21:52:25;  author: dickson;  state: Exp;  lines: +11 -12
placement change to avoid toplevel collisions
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hc/hc_brresp.pla,v
Working file: verilog/bsrc/hc/hc_brresp.pla
head: 65.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 65.2
date: 1995/06/20 21:56:23;  author: woody;  state: Exp;  lines: +24 -14
hc_brresp.pla, hc.h: Simplified event daemon prb processing since it was
possible that the prb repsonse could be granted before ostate loaded the tag
into the sid[7] tag register. This was noticed by standalone test gauntlet
(CPUCLK=13, IOCLK=8). Saves ~70 hopper atoms (as reported by planet).

No placement change required.

Passed multiple standalone tests: gauntlet, termite, hexratio, evnt8
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hc/hc_sid.Veqn,v
Working file: verilog/bsrc/hc/hc_sid.Veqn
head: 3.13
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 13;    selected revisions: 1
description:
----------------------------
```

```
revision 3.12
date: 1995/06/20 05:13:32;  author: woody;  state: Exp;  lines: +2 -2
Only allow tagen[7] when set is active to prevent writing event daemon tag with
bogus value
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/rg/BOM,v
Working file: verilog/bsrc/rg/BOM
head: 136.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 297;   selected revisions: 6
description:
----------------------------
revision 134.0
date: 1995/06/22 18:55:13;  author: dickson;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/rg

avoid toplevel collisions
----------------------------
revision 133.1
date: 1995/06/22 18:55:03;  author: dickson;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 133.0
date: 1995/06/21 21:49:02;  author: dickson;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/rg

placement change to avoid toplevel collisions
----------------------------
revision 132.1
date: 1995/06/21 21:48:53;  author: dickson;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 132.0
date: 1995/06/20 23:55:10;  author: dickson;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/rg

move lower data path section to the right to make room for es growth
----------------------------
revision 131.1
date: 1995/06/20 23:55:00;  author: dickson;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/rg/rg.pim,v
Working file: verilog/bsrc/rg/rg.pim
head: 82.31
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 31;    selected revisions: 3
description:
----------------------------
```

```
revision 82.29
date: 1995/06/22 18:54:22;  author: dickson;  state: Exp;  lines: +1 -1
avoid toplevel collisions
----------------------------
revision 82.28
date: 1995/06/21 21:47:56;  author: dickson;  state: Exp;  lines: +8 -8
placement change to avoid toplevel collisions
----------------------------
revision 82.27
date: 1995/06/20 23:53:58;  author: dickson;  state: Exp;  lines: +1 -1
moved lower data path section to the right of
clock spar to make rome for es growth.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/BOM,v
Working file: verilog/bsrc/uu/BOM
head: 218.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 480;   selected revisions: 2
description:
----------------------------
revision 211.0
date: 1995/06/21 07:33:45;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/uu

uu/uu.V:  Single end many of the instU* and preemdInstU* busses on the bits
  already being forced fullswing by other logic or when halfswing loading
  seemed light enough to not make the power-up risk high.  Rqstd by dickson.
  Explicitly called out vref_0ph in some concatenations so that old .pim works.
----------------------------
revision 210.1
date: 1995/06/21 07:33:36;  author: mws;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/uu.V,v
Working file: verilog/bsrc/uu/uu.V
head: 1.202
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 202;   selected revisions: 1
description:
issue unit
----------------------------
revision 1.197
date: 1995/06/21 07:32:27;  author: mws;  state: Exp;  lines: +71 -35
uu/uu.V:  Single end many of the instU* and preemdInstU* busses on the bits
  already being forced fullswing by other logic or when halfswing loading
  seemed light enough to not make the power-up risk high.  Rqstd by dickson.
  Explicitly called out vref_0ph in some concatenations so that old .pim works.
=============================================================================
```